## **REMARKS**

Claims 1-29 are pending in the above-identified application. The following objections and rejections are respectfully traversed in light of the following remarks, and reconsideration is requested.

Claims 1 and 3-29 were rejected under 35 U.S.C. §103(a) as being unpatentable over Yung (U.S. 5,592,679). In the rejection, the Examiner stated:

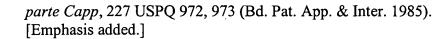
Yung discloses a system having a plurality of processors and a global register which is shared by the processors. Each of the processors further includes its own local register which can be accessed by the associated processor only. The only difference is that Figure 2 of Yung shows a global register represented by a single rectangular box whereas the claims recite a plurality of segments. It is the position of the Examiner that whether register files are physically/logically divided/combined is not a patentable subject matter. Note that the accessibility of the register files by the functional units is the same in both inventions.

Applicants respectfully traverse the Examiner's rejections of Claims 1 and 3-29. The Examiner fails to meet the requirements of MPEP 706.02(j) [Contents of a 35 USC 103 Rejection] which states:

35 USC 103 authorizes a rejection where, to meet the claim, it is necessary to modify a single reference or to combine it with one or more other references....

.... Finally, the prior art reference (or references when combined) must teach or suggest *all claim limitations*. The teaching or suggestion to make the claimed combination and reasonable expectation of success must both be found in the prior art and not based on applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991). See MPEP 2143-2143.03 for decisions pertinent to each of these criteria.

... The initial burden is on the examiner to provide some suggestion of the desirability of doing what the inventor has done. "To support the conclusion that the claimed invention is directed to obvious subject matter, either the references must expressly or impliedly suggest the claimed invention or the examiner must present a convincing line of reasoning as to why the artisan would have found the claimed invention to have been obvious in light of the teachings of the references." Ex



The Examiner has based the rejections of Claims 1 and 3-29 on the position that "whether register files are physically/logically divided/combined is not a patentable subject matter." This position is in direct conflict with the requirements of the MPEP and caselaw. In Claim 1, a register file is divided into a plurality of register file segments; each register file segment being partitioned into a global register file and a local register file. This is structure that Yung does not disclose! Yung teaches separate individual local register files and a shared global file but they are not contained in a single register file segment as is claimed by Applicants! The Examiner refers to Figure 2 and Claim 1 of Yung but Figure 2 shows local register buffer OUTSIDE a single register file segment. Therefore, Applicants respectfully request reconsideration and withdrawal of the rejections to Claims 1 and 3-29 under 35 U.S.C. § 103(a).

The Examiner's position that "whether register files are physically/logically divided/combined is not a patentable subject matter" is without merit and unsupported by any authority, such as the MPEP or caselaw. The Examiner's unsupported position cannot ease the Examiner's required burden of proof in demonstrating that all elements of the claims are disclosed in the reference. See MPEP 706.02(j). By the Examiner's own admission, Yung does not disclose all the elements of the claims since the Examiner has chosen to disregard the structural features found in Claims 1 and 3-29 but not found in Yung. The prior art must disclose the teaching or suggestion to make the claimed combination and a reasonable expectation of success. Yung does not disclose any teaching or suggestion to make the claimed combination. The Examiner is respectfully requested to provide any authority supporting the Examiner's novel and unprecedented position that functional/structural differences between a claim and the prior art are not patentable. The Examiner asserted the

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25 METRO DRIVE SUITE 700 SAN JOSE, CA 95110 (408) 453-9200 FAX (408) 453-7979 same unsupported position during the telephonic interview held on March 2, 2001, between the Examiner, Matthew Spark and Ken Koestner. During the interview, with respect to the rejection of Claim 1, the Examiner stated that he did not believe the structural differences between the references and Claim 1 matters as he believed the references and Claim 1 were equivalent and, in his words, "functionally identical." The Examiner expressed similar comments with respect to Claim 15. When asked, the Examiner repeated his assertion that the structural differences between the references and the claims did not matter as he believed the claims and references to be functionally identical. Then, as now, the Examiner failed to assert any case law or MPEP section to support this unique theory that claimed structure is irrelevant in determining patentability. The Examiner is not authorized to create new rules of patentability; only to examine applications in view of the MPEP and patent law.

Claim 2 was rejected under 35 U.S.C. §103(a) as being unpatentable over Yung (U.S. 5,592,679) in view of Nishimoto (U.S.). In the rejection, the Examiner stated:

Yung discloses claim combination set forth above. Although Yung's processor is of multiple functional units type, it is not clear whether his instructions [sic] are VLIW. VLIW instruction is well-known in the art. Nishimoto shows in Figure 1 a processing system having a local register (line 64, col. 5), in Figure 2 a processing system having a global register (line 35, col. 7). Both systems use VLIW instructions. From the teaching of Nishimoto, it would have been obvious to a person of ordinary skill in the art to use VLIW instructions such that more control signals can be generated.

Applicants traverse the Examiner's rejection of Claim 2 since the combined references fail to show the features of the claimed invention and because there is no suggestion or motivation in the cited references for combining Yung and Nishimoto. As outlined above, Yung does not disclose Claim 1 from which Claim 2 depends. Therefore, Claim 2 is allowable. Arguendo, and without waiver of the above, the Examiner admits that "[a]lthough Yung's processor is of multiple functional units type, it is not clear whether his instrucitons

[sic] are VLIW." Applicants respectfully assert that the Examiner deliberately misconstrues the teaching of Yung in an attempt to bridge the gap between Yung and Nishimoto by stating that "VLIW instruction is well-known in the art." The Examiner admits that Yung does not explicitly teach VLIW yet then contradicts himself a few sentences later by stating the "[b]oth [Yung and Nishimoto] use VLIW instructions." Yung does not disclose the use of VLIW, either explicitly or inherently. The Examiner fails to provide any support for his contention that VLIW is well-known in the art (see MPEP 2144.03) and also fails to set forth what is the ordinary level of skill in the art at the time the invention was made (*Ex parte Hiyamizu*, 10 USPQ 2d 1393, 1394 (BPAI 1988); *Environmental Design, Ltd. v. Union Oil Co.*, 1713 F.2d 693, 697, 218 USPQ 865, 868-9 (Fed. Cir. 1983)). Therefore, Applicants respectfully request reconsideration and withdrawal of the rejection to Claim 2 under 35 U.S.C. § 103(a).

Claims 23-29 were rejected under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. In the rejection, the Examiner stated:

The method as recited is merely a flow chart of an idea to operate a processor. The steps as recited in the claim combination are not actually performed by the processors such that a meaningful result is achieved.

Further, method claim 23 recites a register file as one of the method steps in the claim combination. A claim must be included in one and only one of the four statutory classes of invention. Hybrid claims are not permitted. Ex parte Lyell, 17 USPQ 2<sup>nd</sup> 1548 (BD. PA&I. 1990). In addition, all dependent claims must be of the same type of claim as the parent.

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25 METRO DRIVE SUITE 700 SAN JOSE, CA 95110 (408) 453-9200 FAX (408) 453-7979 In response, Applicants respectfully contend that the above rejection is improper as the Examiner fails to state the basis for the rejection with clearness and particularity. MPEP 2171 states that if "a rejection is based on 35 USC 112, second paragraph, the examiner should further explain whether the rejection is based on indefiniteness or on the failure to claim what 775201 v1/PF-OA [Rev. 000913] -11- Serial No. 09/204,585

applicants regard as their invention. Ex parte Ionescu, 222 USPQ 537, 539 (Bd. App. 1984)." The Examiner fails to provide any explanation as to why the method recited in Claim 23 is rejectable under 35 USC 112, second paragraph (i.e., whether Claim 23 is indefinite or fails to claim what applicants regard as their invention). The Examiner states that "[t]he method as recited is merely a flow chart of an idea to operate a processor." A method claim recites a method of performing a function. A flow chart of the operation of a processor may therefore properly form the basis of a method claim. The Examiner is respectfully requested to provide any authority (e.g., MPEP or caselaw) to the contrary. Claim 23 recites a method of operating a processor; the functions recited in the claim are performed within the processor during the operation of the processor. The 'meaningful result' of the method is the operation of the processor in the manner claimed.

While Ex parte Lyell, 17 USPQ 2nd 1548 (BD. PA&I. 1990) refers to a hybrid claim, Ex parte Lyell is not applicable to Claim 23 as Claim 23 is not a hybrid claim. The Examiner grammatically misconstrues the claim. There is no rule against a method claim reciting structure; the register file is recited structure. Again, the Examiner is respectfully requested to provide any authority to the contrary. To aid the Examiner's comprehension, Claim 23 has been amended in terms of grammar. The scope of Claim 23 remains unchanged.

Claims 1-29 were provisionally rejected under the judicially created doctrine of double patenting over claim 1-22 of copending Application No. 09/204,479 in view of Yung (U.S. 5,592,679). The Examiner stated:

Details of the rejection have already been set forth in the last Office action. The details are incorporated herein by reference thereto.

In the communication filed on April 4, 2001, applicants contended that Yung does not disclose a register file with is divided into a plurality of register file segments which is partitioned into a global register and a local register. The Examiner disagrees. As pointed out in the last Office action,

Figure 2 of Yung clearly shows a plurality of local registers 24nd (n=1-n) each of which is associated with a functional unit (execution pipe) and a global register file (290). Similar to applicants' claimed apparatus, ones of the local register can only be accessed by by ones of the associated execution unit and the global global [sic] register is accessable [sic] by all the functional units. Applicants appear to contend that their Figure 6 shows four separate rectangular boxes labeled as global register files whereas the global register shown in Figure 2 of Yung is represented by a single rectangular box. Firstly, it appears that the four register segments (610-616) shown in Figure 6 is actually a single register file 600. The register files are logically divided and not physically divided. Secondly, it is the position of the Examiner that whether register files are physically/logically divided/combined is not a patentable subject matter. Note that the accessibility of the register files by the functional units is the same in both inventions.

Details of Applicants' response to the combination of Application No. 09/204,479 in view of Yung has already been set forth in the Preliminary Amendment/Response to Final Office Action Dated January 3, 2001 that was mailed April 3, 2001. The details are incorporated herein by reference thereto. As stated above, the Examiner's position that "whether register files are physically/logically divided/combined is not a patentable subject matter" is without merit and unsupported by any authority such as the MPEP or caselaw. For the reasons outlined above, it is improper for the Examiner to ignore structural/functional differences between the claims and alleged prior art. Applicants recognize the provisional nature of the rejections, and will address the need for a terminal disclaimer or other course of action in future communications to this Office should Claims 1-22 of copending Application No. 09/204,479 be allowed at some future point in time and in the same, or substantially the same, form as they now presently exist. Therefore, Applicants respectfully request reconsideration and withdrawal of the rejections to Claims 1-29 under the judicially created doctrine of double patenting.

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## **CONCLUSION**

For the foregoing reasons, Applicant believes the pending Claims 1-29 are allowable, and a Notice of Allowance is respectfully requested. The Examiner is invited to call the Applicants' Attorney at (949) 718-5200 for any questions with this response.

EXPRESS MAIL LABEL NO:

EL849435870US

Respectfully submitted,

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## **ATTACHMENT A**

This response amends claim 23 as follows.

23. (Twice Amended) A method of operating a processor comprising:

providing a processor including a plurality of functional units[;] <u>and</u> a register file divided into a plurality of register file segments, the plurality of register file segments being coupled and associated to ones of the plurality of functional units;

partitioning the register file segments into global registers and local registers; operating the plurality of functional units;

accessing the global registers by the plurality of functional units; and accessing the local registers by the functional unit associated with the register file segment containing the local registers.

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